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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,730	04/13/2004	Shinobu Nohtomi	XA-10079	2939

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KARIMI, PEGEMAN	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
11/30/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
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Office Action Summary	Application No.	Applicant(s)	
	10/822,730	NOHTOMI ET AL.	
	Examiner	Art Unit	
	Pegeman Karimi	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 09/12/2007 has been entered and considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 22-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanatani (U.S. Patent No. 5,414,443) in view of Sakaguchi (U.S. Patent No. 7,006,114).

As to claim 22, Kanatani teaches a method for driving a plurality of pixels (pixels at the intersection of source and gate lines, Fig. 1) in a display panel (100) by a display driver (2) in accordance with a positive phase and a negative phase of a display mode (col. 10, lines 5-7, the method comprising:

inputting display data (Digital Video Signal) to a first driver in the display driver (2);

converting the display data into first display data (first amplitude in Fig. 17(c)) in the positive phase (Vc is in the positive amplitude) and into second display data (second amplitude in Fig. 17(c)) in the negative phase (Vc is in the negative amplitude) using a

converting circuit (77, converts the power source into a negative and positive voltage $-V_0 - -V_7$ and $+V_0 - +V_7$) in the display driver (2) in response to a switching signal (79).

generating a plurality of gradation voltages (col. 12, lines 41-43) using a gradation voltage generating (77) circuit in the display driver (2);

generating (counter electrode drive 8 generates common voltage signals, Fig. 12) a first common voltage in the positive phase (Fig. 17(b) the first amplitude is the first positive voltage) and a second common voltage, different from the first common voltage (the second common voltage is negative , which is different than the first positive common voltage), in the negative phase (Fig. 17(b), the second amplitude is the negative common voltage) using a common voltage driver (8) in the display driver (1), wherein the first and the second common voltage is applied to a common electrode of the plurality of pixels in the display panel (col. 12, lines 58-62);

selecting, using a selector (55) in the display driver (2), a first gradation voltage ($-V_0 - -V_7$, Fig. 17(a)) from the plurality of gradation voltages ($\pm V_0 - \pm V_7$)based on the first display data (first amplitude in Fig. 17(c)) in the positive phase (first amplitude of Vc in Fig. 17(b), which is in the positive phase) and a second gradation voltage ($+V_0 - +V_7$) from the plurality of gradation voltages ($\pm V_0 - \pm V_7$) based on the second display data (second amplitude in Fig. 17(c)) in the negative phase (second amplitude of Vc in fig. 17(b), which is in the negative phase), wherein the first and the second gradation

voltages are applied to a pixel electrode (col. 12, lines 48-53) of a selected pixel of the plurality of pixels in the display panel (pixels at the intersection of source and gate lines);

in the positive phase (Fig. 17(b), first positive amplitude of Vc), providing the first gradation voltage (Fig. 17(a), $-V_0 - -V_7$) and the first common voltage (Fig. 17(b), at the interval of $-V_0 - -V_7$, the first common voltage is applied) to the display panel ; and in the negative phase (second amplitude, which is negative phase of Vc), providing the second gradation voltage (Fig. 17(a), $+V_0 - +V_7$) and the second common voltage to the display panel (Fig. 17(b), at the interval of $+V_0 - +V_7$, the second common voltage is applied).

Kanatani does not mention the display data are in the same bit pattern.

Sakaguchi teaches the first display data (Gradation display use data, from 00H-1FH) and the second display data (from 20H-3FH) are in the same bit pattern except for one specified bit (the bits of the gradation display use data are in the same bit pattern, e.g. 00H is in the same bit pattern as 20H, the difference is in MSB) when converting the display data (37, col. 11, lines 12-15; col. 15, lines 12-19). Therefore it would have been obvious to one of ordinary skilled in the art at the time the invention was made to have added the digital display data for selecting gradation voltage of Sakaguchi to the display device of Kanatani because the display data for selecting gradation voltages of

Sakaguchi would provide reduction in power consumption of the driving circuit and miniaturization of a driving circuit (col. 6, lines 1-8 of Sakaguchi).

As to claim 27, Kanatani teaches a display system (1) comprising:

a display panel (100) including a plurality of signal lines (102), a plurality of scanning lines (101), a common electrode (105), a plurality of pixels coupled to the plurality of signal lines (pixels are at the intersection of the source lines and gate lines and connected to common electrodes), the plurality of scanning lines (gate lines), and the common electrode (105) so that one pixel is coupled to one signal line, one scanning line, and the common electrode (fig. 1, 100),

wherein one pixel includes a MOSFET (104) having a gate coupled to one scanning line (the gate lines is connected to the gate lines 101) and a source-drain path coupled between one signal line and a pixel electrode opposite to the common electrode (source-drain of 104 is connected between the gate line 101 and 103);

a display driver (2) coupled to the plurality of signal lines (102), the plurality of scanning lines (101), and the common electrode (105), wherein the display driver comprises:

a gradation voltage generator (7) providing a plurality of gradation voltages (col. 10, lines 2-7);

a first driver (2) coupled to the plurality of signal lines (102) and including:
a converting circuit (77) coupled to receive display data (circuit 77 is coupled to source driver, which receives signals from a digital video signal) and responsive to a switching

signal (79) which controls a switching of a positive phase and a negative phase (col. 11, lines 37-47), and which provides first data (first amplitude in Fig. 17(c)) in the positive phase (Vc is in the positive amplitude) and second data (second amplitude of Fig. 17(c)) in the negative phase (Vc is in the negative amplitude)

selectors (55, $AG_0 - AG_7$) coupled to receive the plurality of gradation voltages ($\pm V_0 - \pm V_7$) and to select ones of the plurality of gradation voltages for the plurality of signal lines (col. 11, lines 37-47), respectively, in response to the first and the second data (first and second amplitude in Fig. 17(c));

a second driver (3) coupled to the plurality of scanning lines (101) and which outputs a selection signal to sequentially select one of the plurality of scanning lines (col. 1, lines 51-52); and

a third driver (8) coupled to the common electrode (105) and which provides, to the common electrode, a first common voltage (e.g. $+V_3 - +V_7$) in the positive phase and which provides, to the common electrode, a second common voltage (e.g. $-V_3 - -V_7$) different from the first common voltage in the negative phase (Fig. 17(a) and (b)), (col. 10, lines 2-15). Kanatani does not mention the display data are in the same bit pattern.

Sakaguchi teaches the first display data (Gradation display use data, from 00H-1FH) and the second display data (from 20H-3FH) are in the same bit pattern except for one specified bit (the bits of the gradation display use data are in the same bit pattern, e.g. 00H is in the same bit pattern as 20H, the difference is in MSB) when converting the display data (37, col. 11, lines 12-15; col. 15, lines 12-19);

As to Claim 34, this claim differs from claim 27 only in that the limitations "a display driver on a semiconductor substrate" and "a display memory, which stores display data" are additionally recited. The limitation "a display driver on a semiconductor substrate" is well known in the art. Kanatani teaches a display memory (30), which stores display data (col. 8, lines 47-53).

As to claims 23, 28, and 35, Sakaguchi teaches the one specified bit (Most Significant Bit) is the highest order bit (see col. 17, Table 1).

As to claims 24, 29, and 36. Sakaguchi teaches when the switching signal (col. 13, lines 19-37) is at a level corresponding to logic 0 (col. 13, line 30), the highest order bit (Table 1, Most significant bit) of the display data is the same as that of the first display data (table 1, 20H-3FH), wherein when the switching signal is at a level corresponding to logic 1 (col. 13, line 35), the highest order bit (Table 1, Most significant bit) of the display data is inverted and allocated (col. 13, lines 34-38) as the highest order bit of the second display data (00H-1FH),
wherein when the highest order bit (Table 1, MSB) of the display is at a level corresponding to logic 1 (col. 16, lines 12-13), the lower order bits of the first display data and the second display data are the same as the lower order bits of the display data (the bits of the gradation display use data are in the same bit pattern, e.g. 00H is in the same bit pattern as 20H, the difference is in MSB), and

wherein when the highest order bit is at a level corresponding to logic 0 (col. 16, line 20), the lower order bits (table 1, bit 0- bit 4) of the display data (gradation display use data) is inverted and allocated as the lower order bits of the first display data and the second display data (col. 13, line 32 and line 37), ($\pm V_0 - \pm V_{63}$).

As to claim 25, Kanatani teaches the display driver (2) further comprises a RAM (34), and wherein, in said inputting, the display data is provided from the RAM to the first driver (col. 14, lines 1-3).

As to claim 26, Sakaguchi teaches wherein, in said inputting, the display data is provided from a microcomputer (4), (col. 8, lines 32-33).

As to claim 30, Kanatani teaches the display driver (2) further comprises a display memory (34) which provides the display data (col. 14, lines 1-3).

As to claims 31 and 32, the limitation "the display driver is on a semiconductor substrate" is well known in the art.

As to claim 33, Sakaguchi teaches a microcomputer (4) which provides the display data (col. 8, lines 32-33).

Response to Arguments

4. Applicant's arguments filed on 09/12/2007 have been fully considered but they are not persuasive.

In view of amendment adding new claims 22-36, the references Kanatani and Sakaguchi are used.

On Page 12, Applicant states that the priority documents were attached to the submission of priority document filed on June 15, 2004, however, the documents have not been received. The documents are either lost or not attached to the letter of "submission of priority documents". Applicant is requested to resubmit the priority documents. So that they can fully comply and claim for foreign priority under 35 U.S.C 119(a)-(d).

On page 13, paragraph 4, applicant argues that Kanatani does not teach or suggest among other features, display data is converted into first display data in the positive phase and into second display data in the negative phase using a converting circuit in response to a switching signal so that the first display data and the second display data are in the same bit Patten except for one specified bit when converting the display data. Kanatani teaches converting the display data, which is inputted from a Digital Video Signal to the source driver, with element 77 that converts the power source into positive and negative voltage in response to a switching element 79 into positive and negative display data as can be seen in Fig. 17(c).

On Page 14, paragraph 2, applicant argues that Sakaguchi merely discloses that the operation of the operational amplifier is based on the MSB of the display data. Sakaguchi teaches output from the converting sections 371 and 372 of the D/A conversion unit 37 is supplied to output circuit 38 and then supplied to the output terminals 40 of the display device. The D/A conversion unit 37 selects one of the inputted standard voltages in sixty four levels, which thirty two levels for each of the D/A converting sections 371-372).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquires

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pegeman Karimi whose telephone number is (571) 270-1712. The examiner can normally be reached on Monday-Thursday 8:00am - 5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pegeman Karimi
11/26/2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER